

NON-VOLATILE MEMORY INTEGRATED CIRCUIT

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ABSTRACT

A nonvolatile memory integrated circuit arrayed in rows and columns is disclosed. Parallel lines of implant N-type regions are formed in a P-well of a semiconductor substrate, with lines of oxide material isolating each pair of the lines. Columns of memory cells straddle respective pairs of the implant region lines, with one line of the pair forming the source region and one line of the pair forming the drain region of each memory cell of the column. Each memory cell has a floating polysilicon storage gate. One of plural wordlines overlies each row of the memory cells. The portion of the wordline overlying each memory cells forms the control gate of the memory cell. Programming and erase operations occur by Fowler-Nordheim tunneling of electrons through a tunnel oxide layer between the floating gate and the source of the cell.